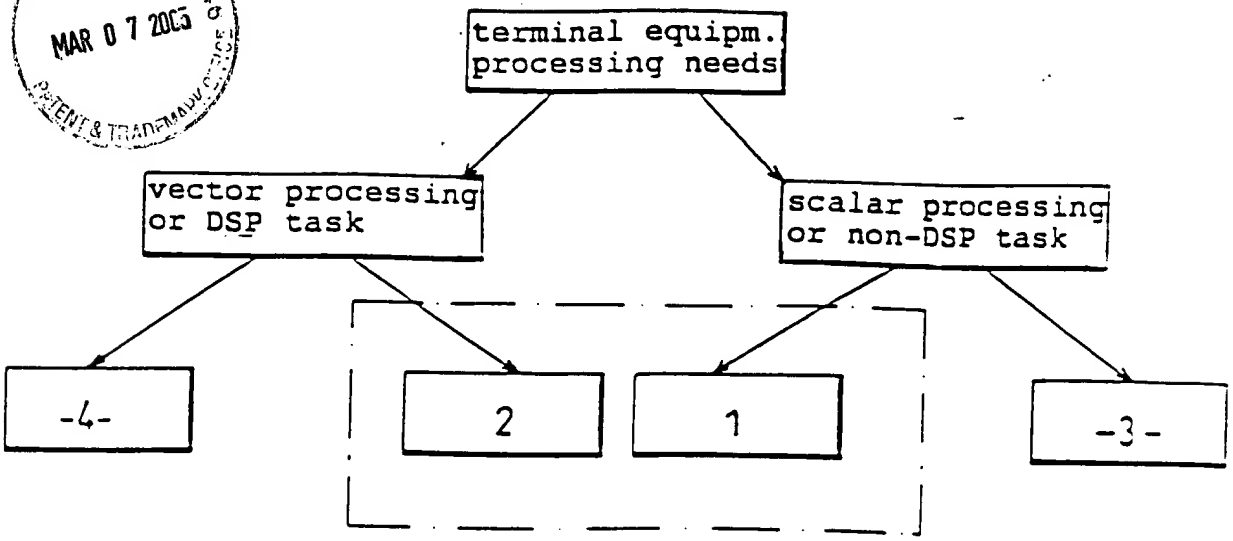
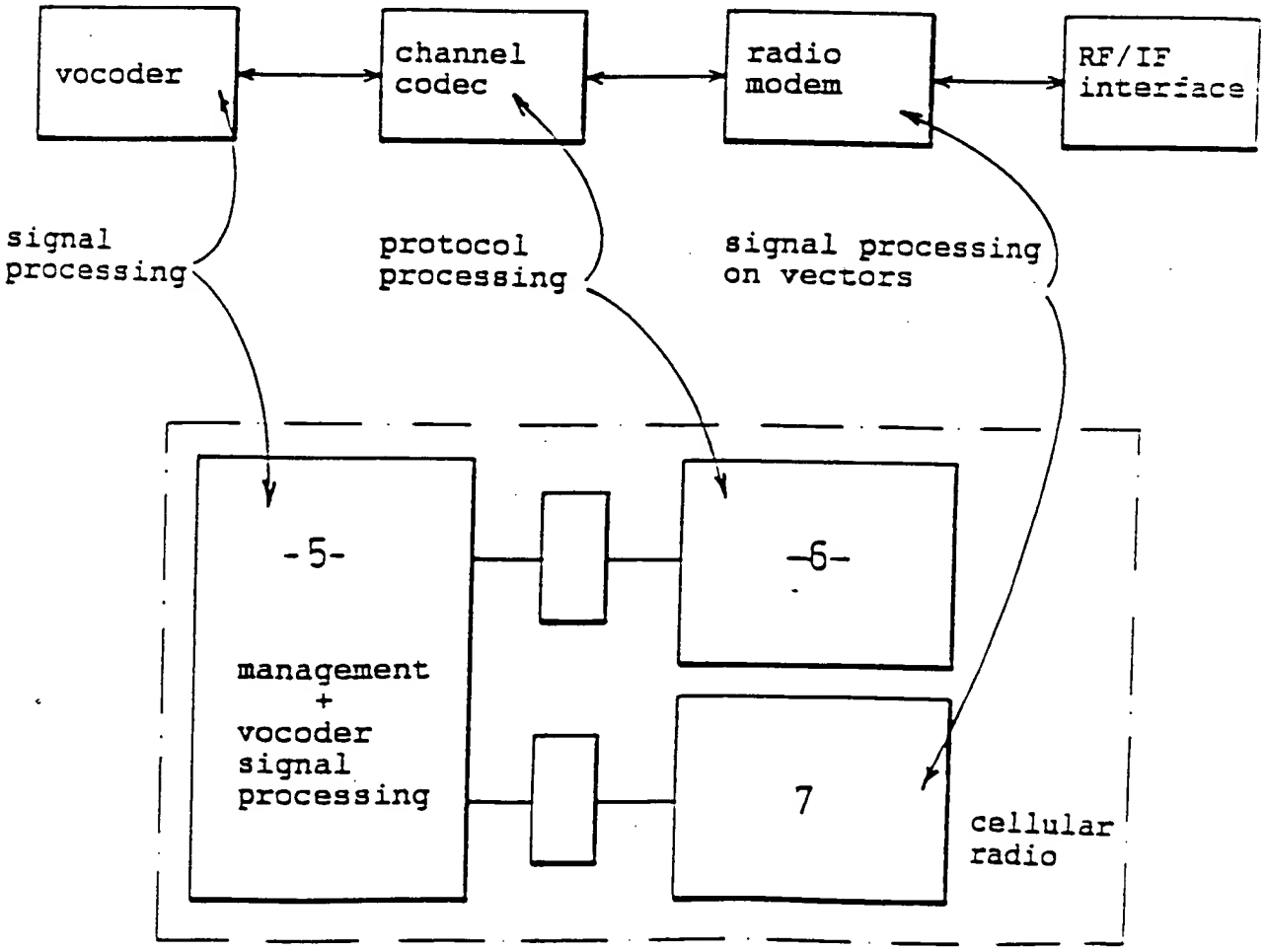


FIG·1



FIG·2

PERFORMANCE OF CHANNEL CODEC ROUTINES

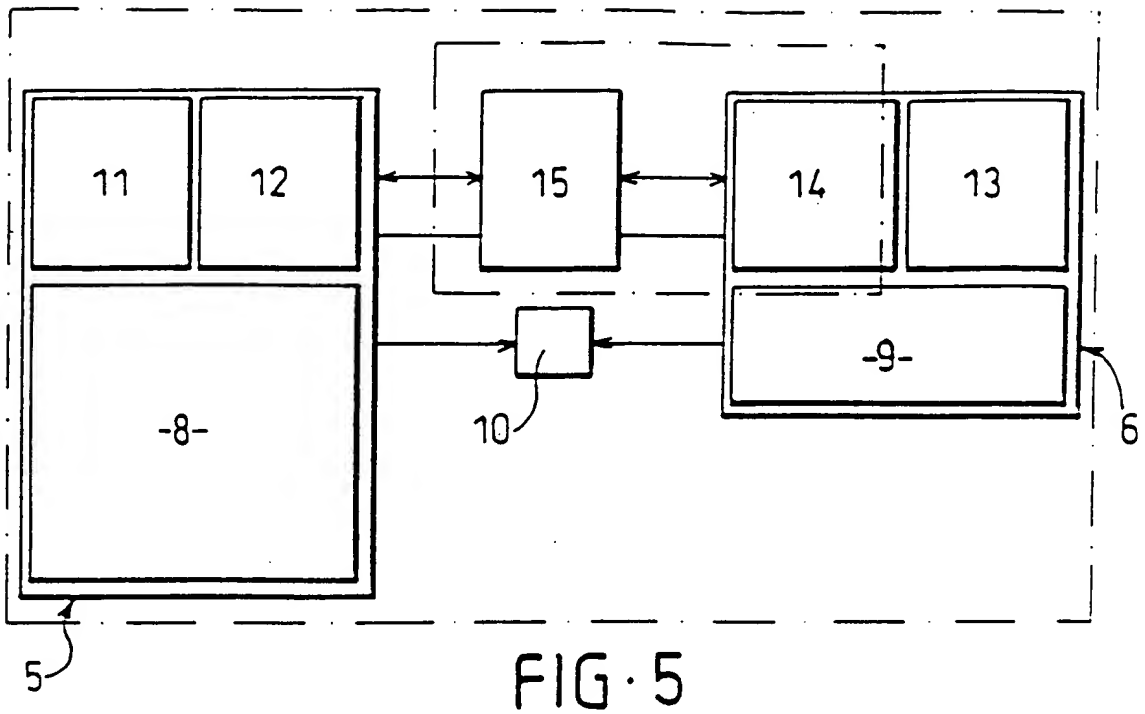
routines	DSP C5x utilisation	proc. protocol PP utilisation
16 bit CRC	6 instr/ bit	4 instr/ bit
identification	5 instr/ bit	1 instr/ bit
RATIO		
sel/instr efficiency	×1	×2,2
no. of trans.	58 KTx	6,5 KTx
MIPS	28 MIPS	28×2,2=62 MIPS DSP

FIG·3

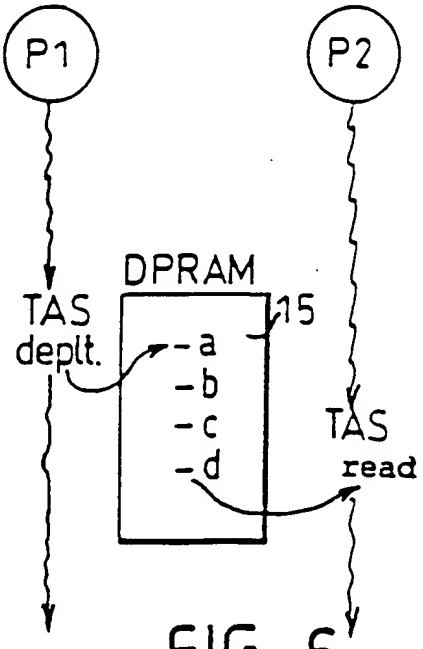
PERFORMANCE OF MODEM ROUTINES

routines	DSP C5x utilisation	array proc.
metric computation		
57 symbols	43800 cycles	4400 cycles
(4 samples)		
RATIO		
instruction setting efficiency	×1	×10
MIPS	28 MIPS	28×10=280 MIPS DSP

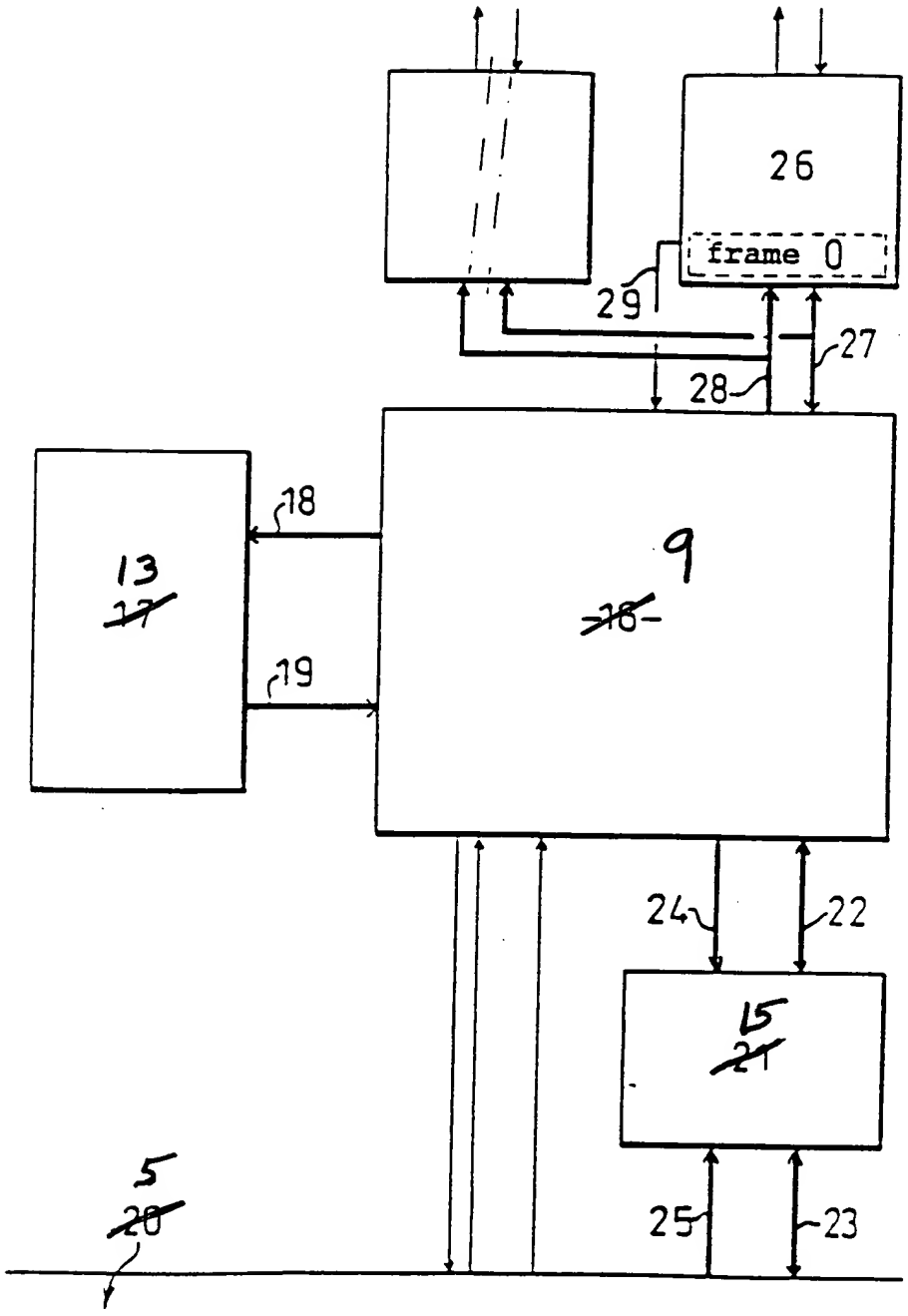
FIG·4



FIG·5



FIG·6



FIG·7

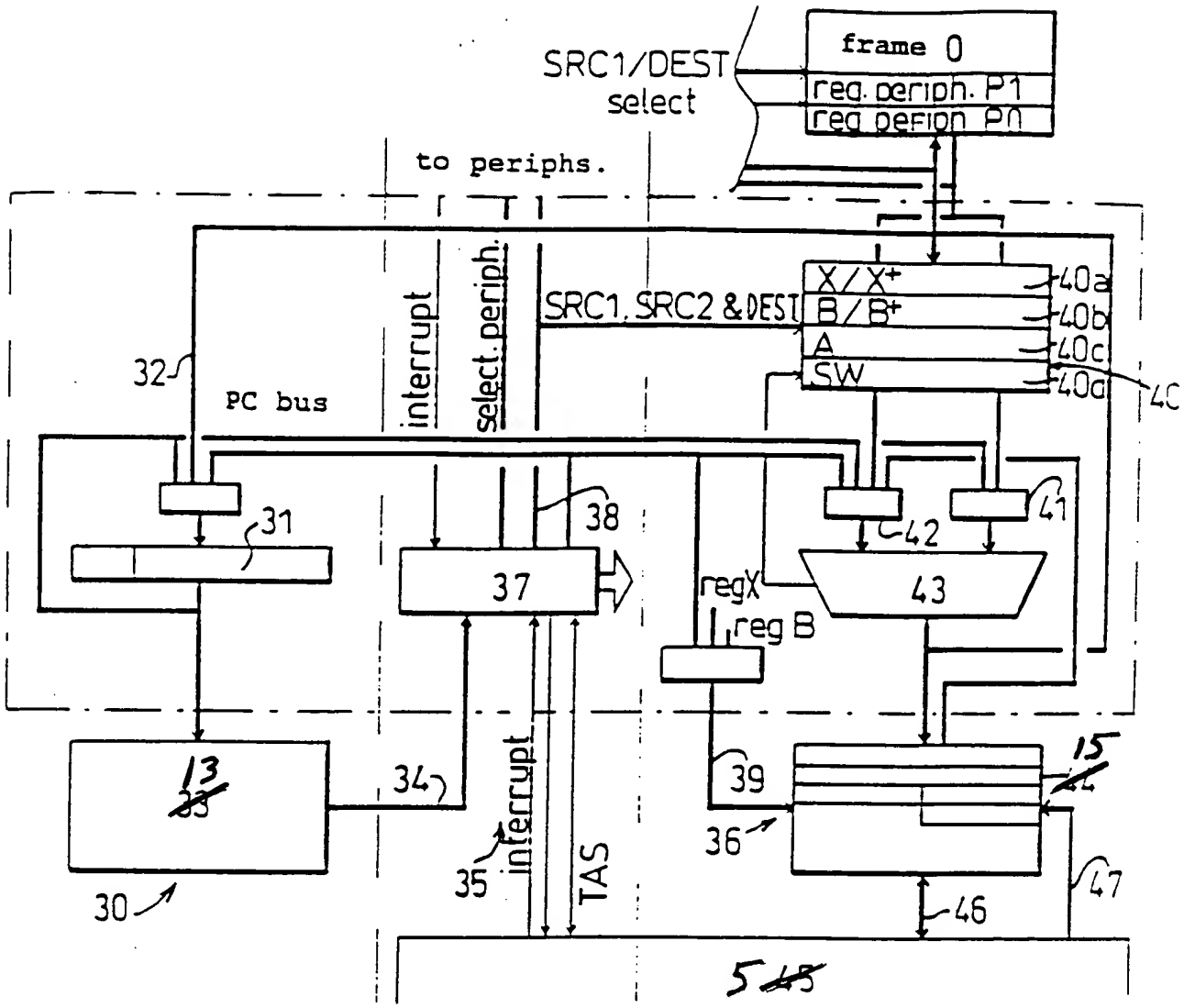

SRC1/DEST
select
frame 0
reg. periph. P1
reg. periph. PN
to periphs.
interrupt
select. periph.
SRC1, SRC2 & DEST
X / X+
B / B+
A
SW
40a
40b
40c
40d
40
32
PC bus
31
38
37
42
41
43
regX
reg B
13
34
39
15
36
35
interrupt
TAS
47
46
30
5

FIG · 8

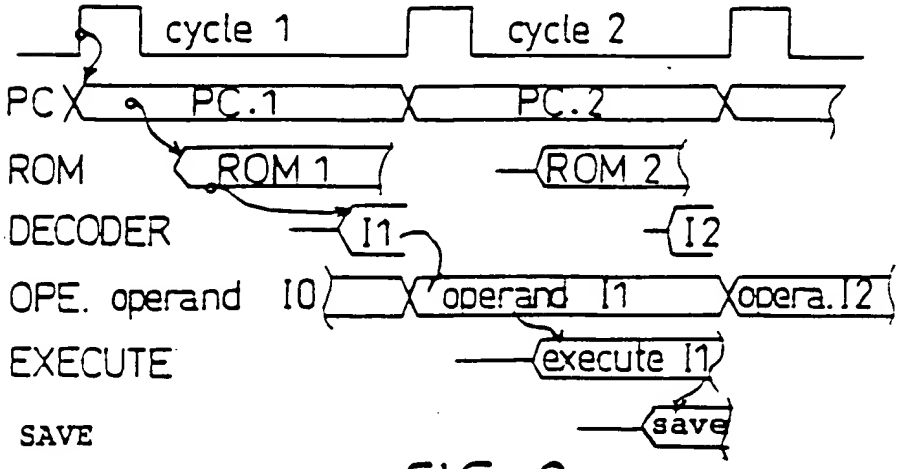

cycle 1
cycle 2
PC
PC.1
PC.2
ROM
ROM 1
ROM 2
DECODER
I1
I2
OPE. operand
I0
operand I1
opera. I2
EXECUTE
execute I1
SAVE
save

FIG · 9

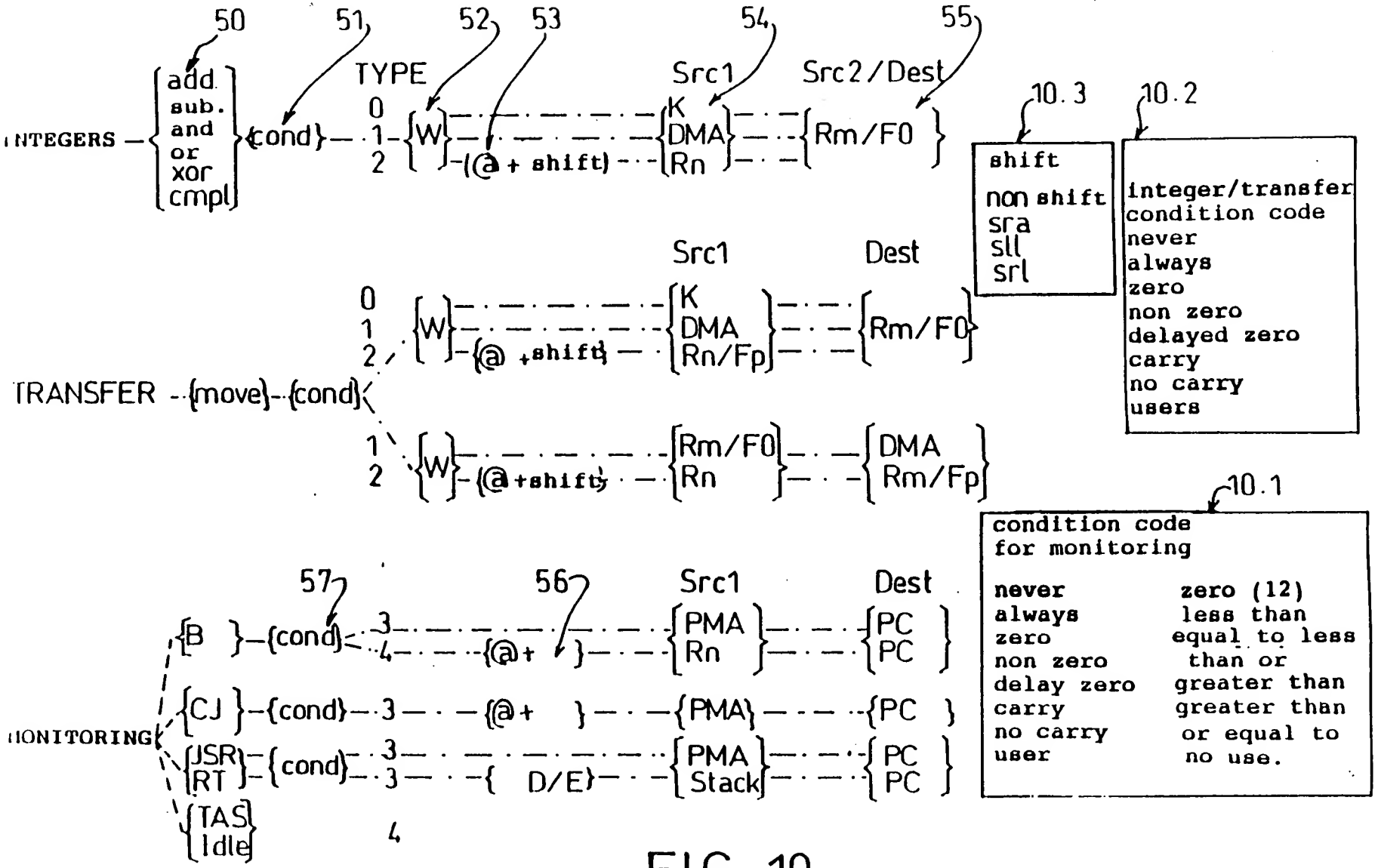
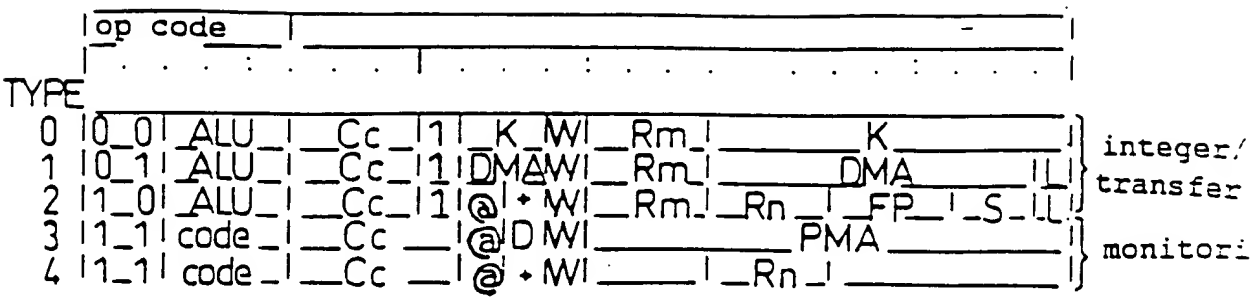

50
51
52
53
54
55
TYPE
Src1
Src2/Dest
INTEGERS
add
sub.
and
or
xor
cmpl
{cond}
0
1
2
W
(@ + shift)
K
DMA
Rn
Rm/F0
10.3
shift
non shift
sra
sll
srl
10.2
integer/transfer condition code
never
always
zero
non zero
delayed zero
carry
no carry
users
Src1
Dest
TRANSFER
{move}
{cond}
0
1
2
W
(@ +shift)
K
DMA
Rn/Fp
Rm/F0
1
2
W
(@+shift)
Rm/F0
Rn
DMA
Rm/Fp
10.1
condition code for monitoring
never
always
zero
non zero
delay zero
carry
no carry
user
zero (12)
less than
equal to less than or
greater than
greater than or equal to
no use.
57
56
Src1
Dest
MONITORING
{B }
{CJ }
{JSR RT}
{TAS Idle}
{cond}
3
4
(@+ D/E)
PMA
Rn
Stack
PC
PC
PC
PC
4

FIG · 10

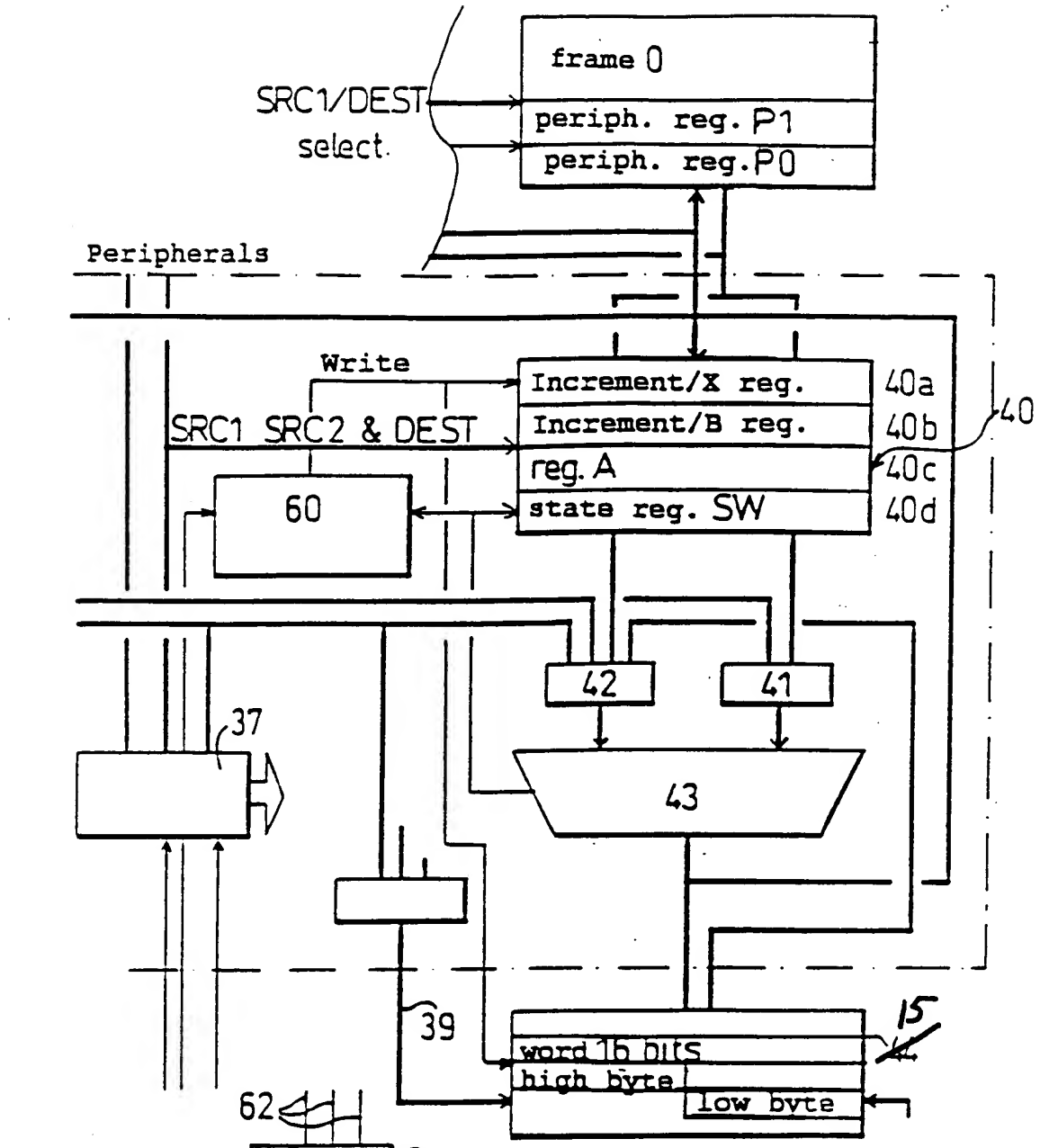


FIG·11

ALU	Code	Cc	
0 - sub	0 - ST type 1	0 - never	8 - Z12
1 - CPL	1 - ST type 2	1 - always	9 - LO
2 - add	2 - B type 3	2 - Z	10 - LE
3 - and	3 - B type 4	3 - NZ	11 - G
4 - or	4 - CALL	4 - ZD	12 - GE
5 - XOR	5 - RTS	5 - C	13 - NU
6 - PASSA	6 - RTI	6 - NC	14 - (BL)
7 - SUBC	7 - STOP	7 - user	15 -

Rm/Rn	W	L	S
0 - P0	0 - R/W byte	--> 0 - Rm low	0 - PASS
1 - P1	1 - R/W word	1 - Rm high	1 - SRA
2 - A			2 - SLL
3 - B			3 - SRL
4 - X			
5 - PC		L	
6 - SW			
7 - SP		--> 0 - DMA/Rn low	
		1 - DMA/Rn high	

FIG·12


frame 0
SRC1/DEST
select
periph. reg. P1
periph. reg. P0
Peripherals
Write
Increment/X reg.
40a
SRC1 SRC2 & DEST
Increment/B reg.
40b
40
reg. A
40c
60
state reg. SW
40d
42
41
37
43
39
15
word 16 bits
high byte
low byte
62
61
never
always
zero
non zero
delay zer
carry
no car.
user
write reg.
memory write
WE
state reg. SW cond bits

FIG·13

FIG·14

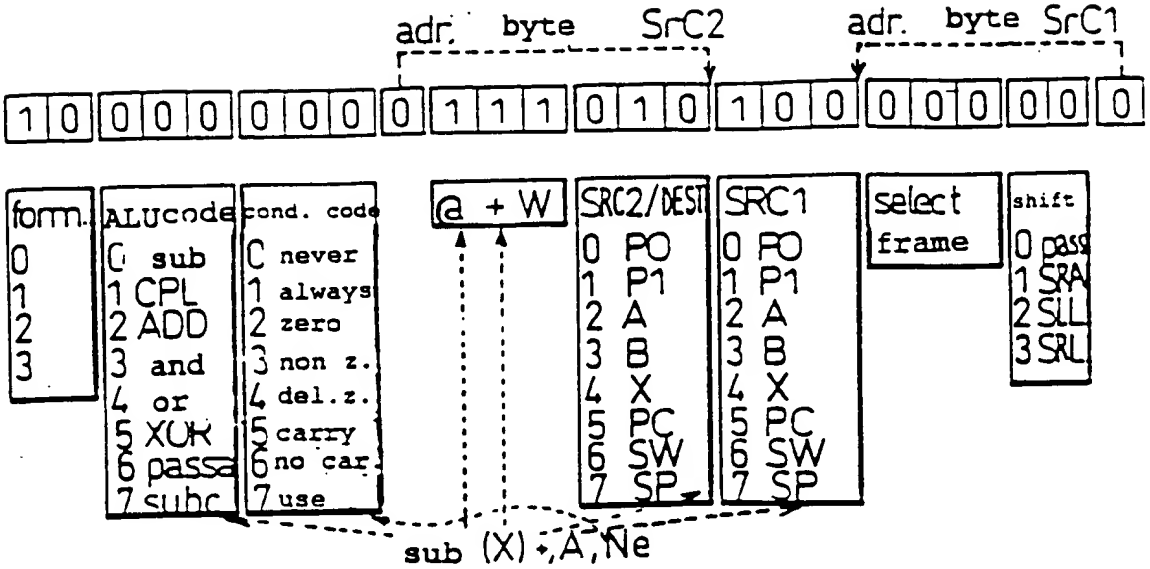

adr. byte SrC2
adr. byte SrC1
1 0 0 0 0 0 0 0 0 1 1 1 0 1 0 1 0 0 0 0 0 0 0 0
form.
0
1
2
3
ALUcode
0 sub
1 CPL
2 ADD
3 and
4 or
5 XOR
6 passa
7 subc
cond. code
0 never
1 always
2 zero
3 non z.
4 del.z.
5 carry
6 no car.
7 use
@ + W
SRC2/DEST
0 P0
1 P1
2 A
3 B
4 X
5 PC
6 SW
7 SP
SRC1
0 P0
1 P1
2 A
3 B
4 X
5 PC
6 SW
7 SP
select frame
shift
0 pass
1 SRA
2 SLL
3 SRL
sub (X) ÷, A, Ne

FIG.15

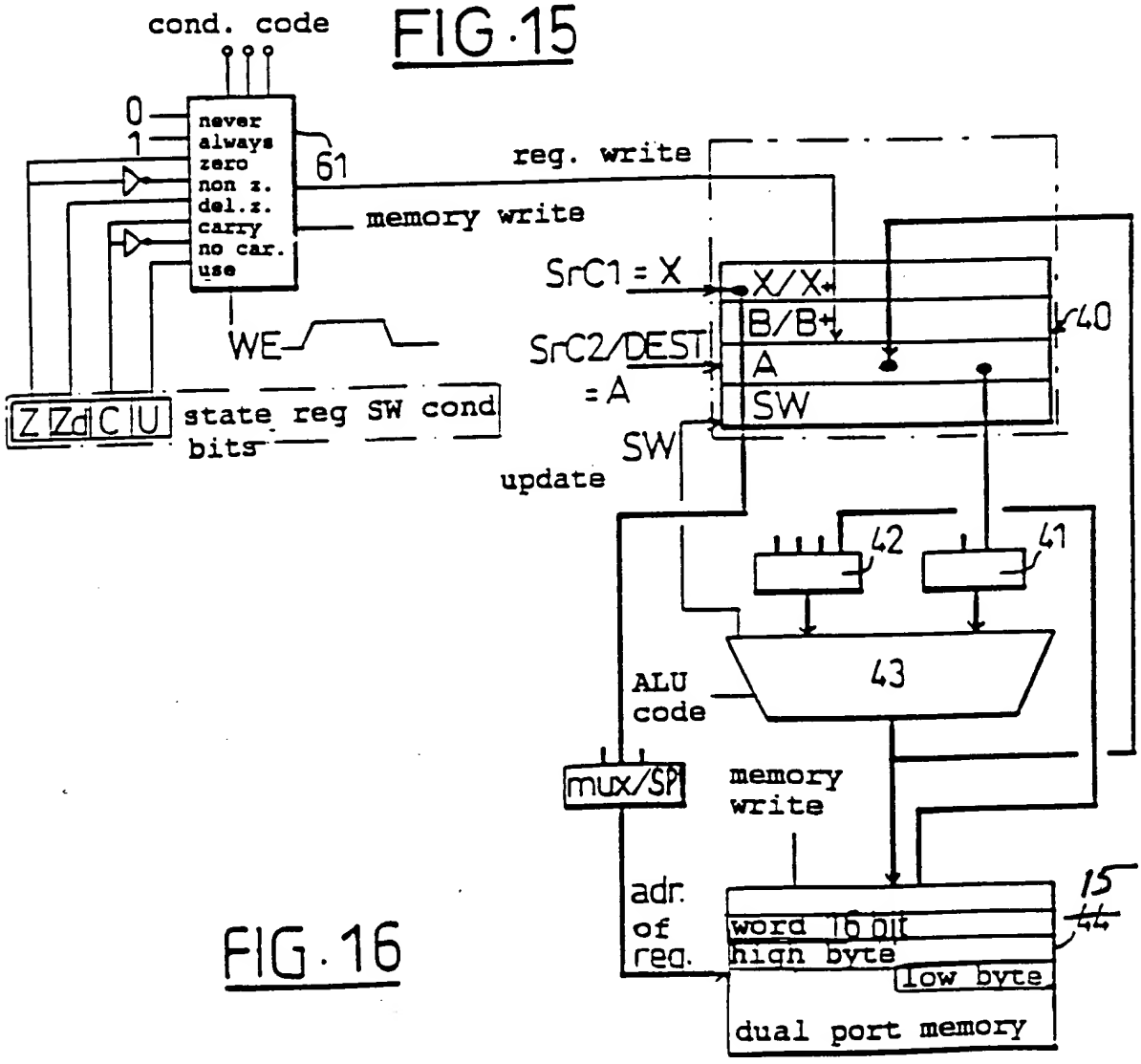

cond. code
0
1
never
always
zero
non z.
del.z.
carry
no car.
use
61
reg. write
memory write
WE
Z Zd C U
state reg SW cond bits
SrC1 = X
SrC2/DEST = A
X/X
B/B
A
SW
40
SW update
42
41
43
ALU code
mux/SP
memory write
adr. of reg.
word 16 bit
high byte
low byte
dual port memory
15
44

FIG.16

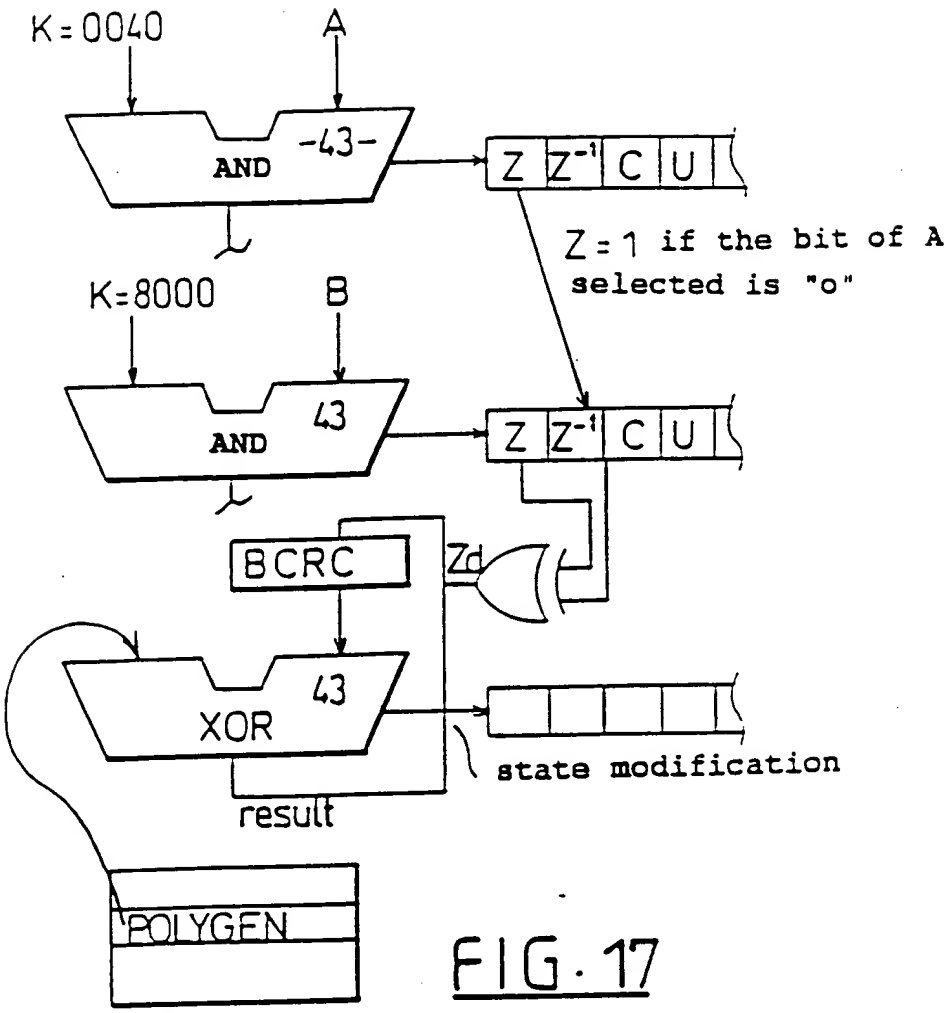

K=0040
A
AND
-43-
Z
Z-1
C
U
Z=1 if the bit of A selected is "o"
K=8000
B
AND
43
Z
Z-1
C
U
BCRC
Zd
XOR
43
state modification
result
POLYGEN

FIG.17

REPLACEMENT SHEET

FIG. 1

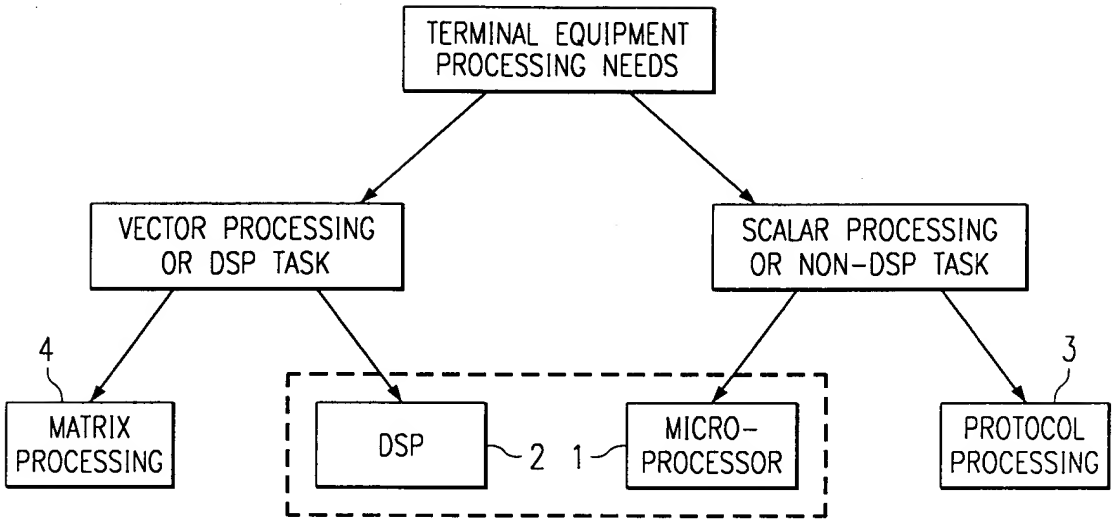


FIG. 2

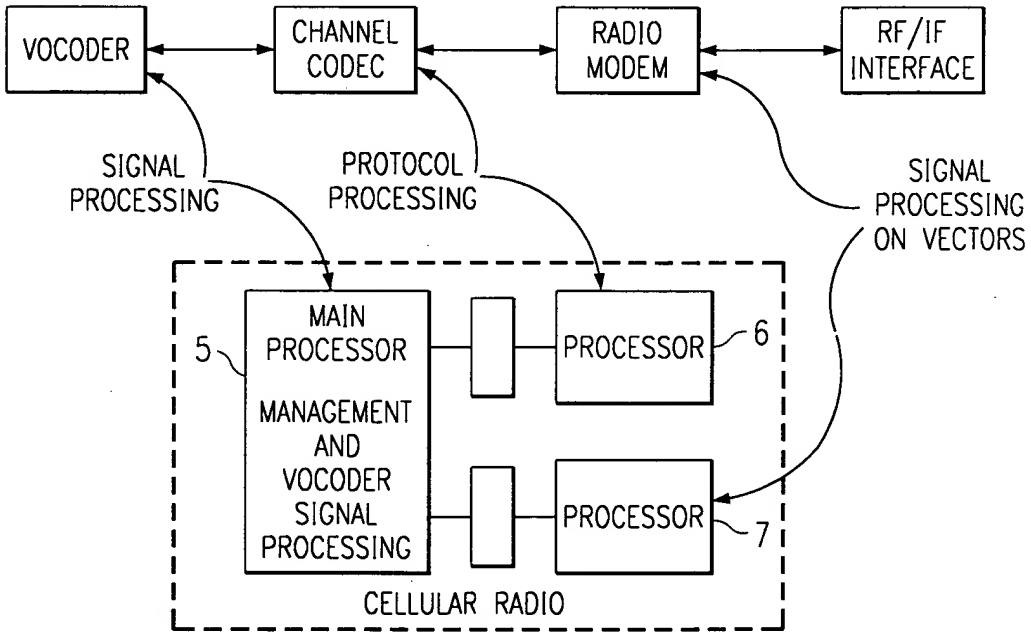


FIG. 3

PERFORMANCE OF CHANNEL CODEC ROUTINES

ROUTINES	DSP UTILIZATION C5x	PROC PROTOCOL PP UTILIZATION
16 BIT CRC	6 INSTR/BIT	4 INSTR/BIT
IDENTIFICATION	5 INSTR/BIT	1 INSTR/BIT

RATIO		
SEL/INSTR EFFICIENCY	x1	x2.2
NO. OF TRANS	58 KTx	6.5 KTx
MIPS	28 MIPS	28x2.2=62 MIPS DSP

FIG. 4

PERFORMANCE OF MODEM ROUTINES

ROUTINES	DSP UTILIZATION C5x	ARRAY PROC
METRIC COMPUTATION 57 SYMBOLS (4 SAMPLES)	43800 CYCLES	4400 CYCLES

RATIO		
INSTRUCTION SETTING EFFICIENCY	x1	x10
MIPS	28 MIPS	28x10=280 MIPS DSP

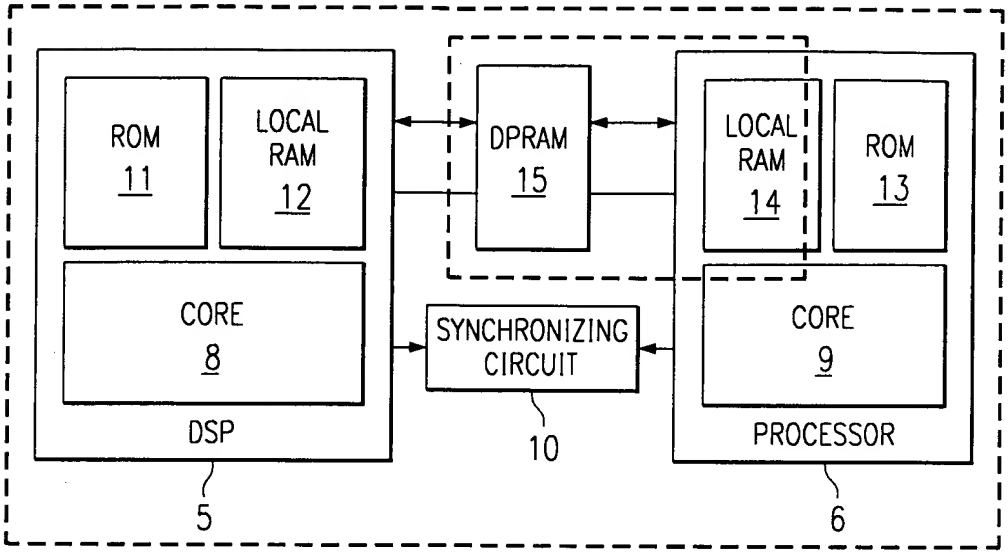


FIG. 5

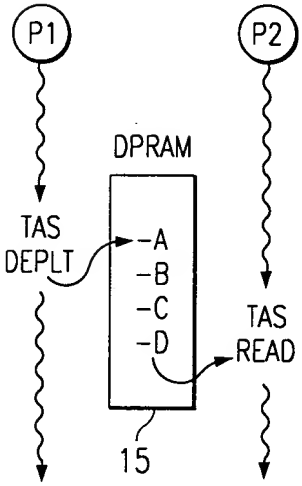


FIG. 6

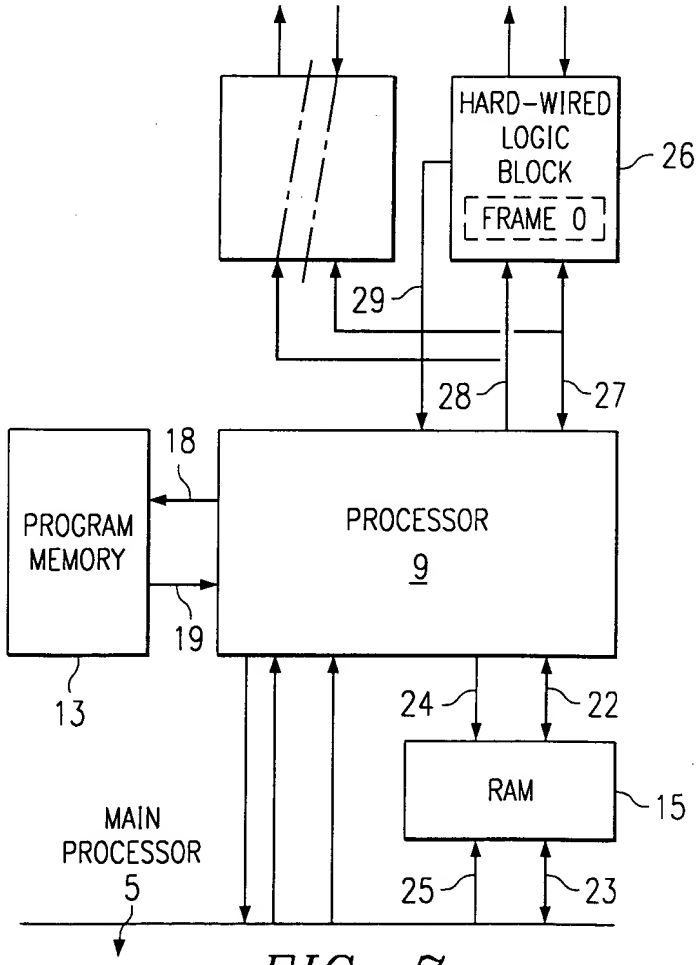


FIG. 7

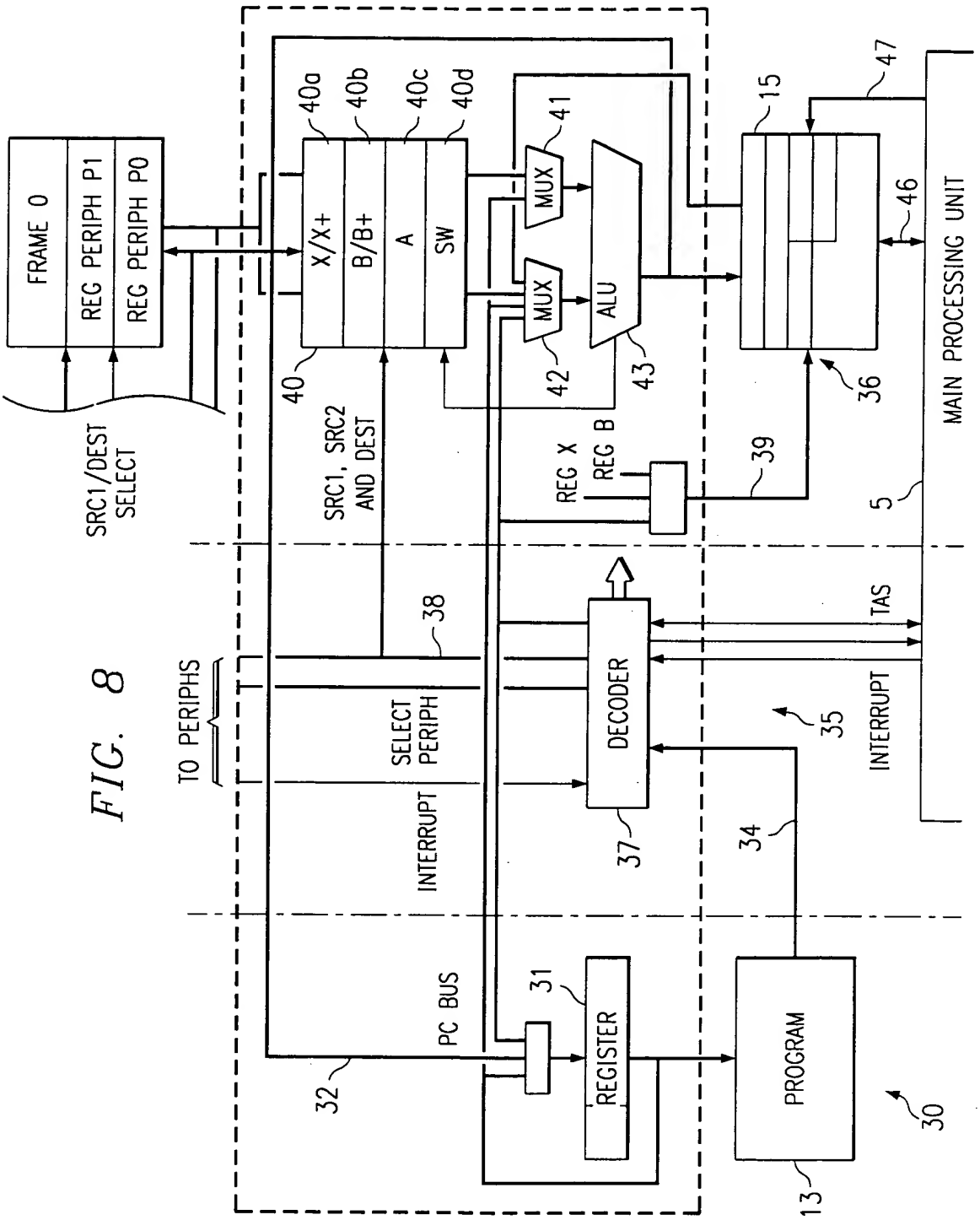

FRAME 0
REG PERIPH P1
REG PERIPH P0
SRC1/DEST SELECT
40a
40b
40c
40d
X/X+
B/B+
A
SW
40
SRC1, SRC2 AND DEST
MUX
MUX
41
42
ALU
43
REG X
REG B
39
15
47
46
36
MAIN PROCESSING UNIT
5
TO PERIPHS
38
SELECT PERIPH
INTERRUPT
DECODER
37
TAS
INTERRUPT
35
34
PC BUS
31
REGISTER
32
PROGRAM
13
30

FIG. 8

FIG. 9

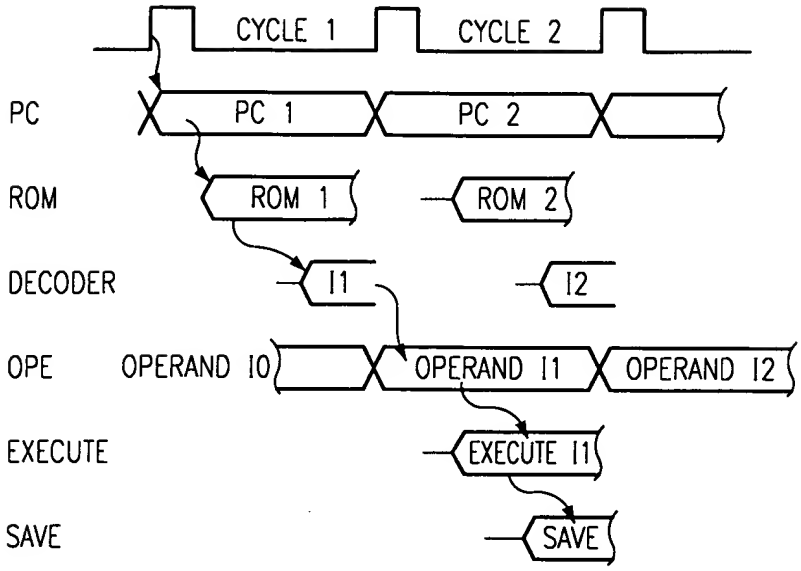


FIG. 11

	OP CODE												
TYPE													
0	0 0	ALU	Cc	1	K		W	Rm	K				INTEGER/ TRANSFER
1	0 1	ALU	Cc	1	DMA		W	Rm	DMA			L	
2	1 0	ALU	Cc	1	@	+	W	Rm	Rn	FP	S	L	
3	1 1	CODE	Cc		@	D	W	PMA					MONITORING
4	1 1	CODE	Cc		@	+	W		Rn				

FIG. 10

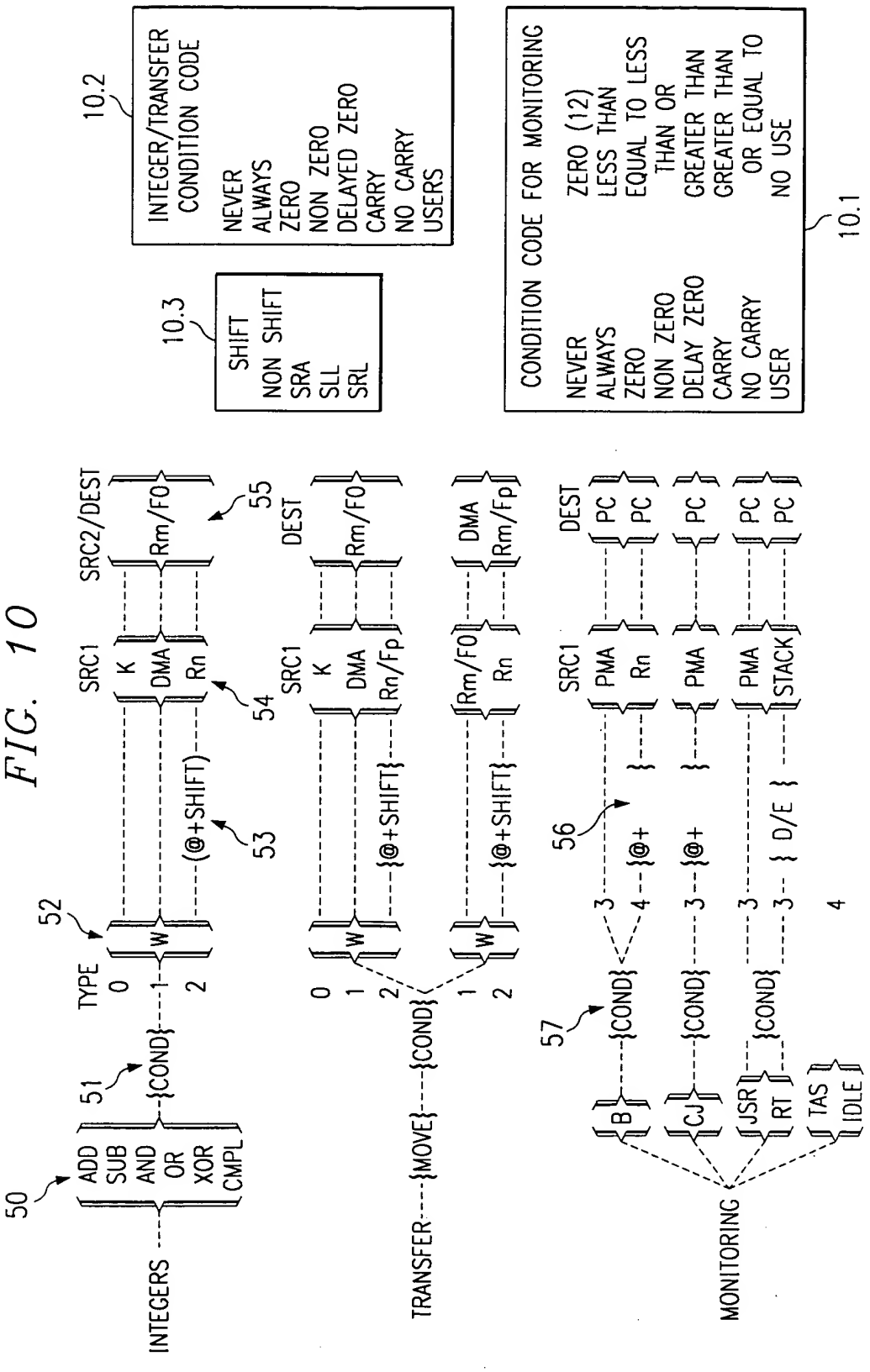

10.2
INTEGER/TRANSFER CONDITION CODE
NEVER
ALWAYS
ZERO
NON ZERO
DELAYED ZERO
CARRY
NO CARRY
USERS
10.3
SHIFT
NON SHIFT
SRA
SLL
SRL
CONDITION CODE FOR MONITORING
NEVER
ALWAYS
ZERO
NON ZERO
DELAY ZERO
CARRY
NO CARRY
USER
ZERO (12)
LESS THAN
EQUAL TO LESS THAN OR
GREATER THAN
GREATER THAN OR EQUAL TO
NO USE
10.1
50
51
52
53
54
55
56
57
INTEGERS
ADD
SUB
AND
OR
XOR
CMPL
{COND}
TYPE
SRC1
SRC2/DEST
K
DMA
Rn
Rm/F0
(@+SHIFT)
TRANSFER
{MOVE}
DEST
Rn/Fp
DMA
Rm/Fp
MONITORING
PMA
PC
STACK
B
CJ
JSR
RT
TAS
IDLE
{@+
D/E

FIG. 12

ALU
0 - SUB
1 - CPL
2 - ADD
3 - AND
4 - OR
5 - XOR
6 - PASSA
7 - SUBC

CODE
0 - ST TYPE 1
1 - ST TYPE 2
2 - B TYPE 3
3 - B TYPE 4
4 - CALL
5 - RTS
6 - RTI
7 - STOP

Cc	
0 - NEVER	8 - Z12
1 - ALWAYS	9 - LO
2 - Z	10 - LE
3 - NZ	11 - G
4 - ZD	12 - GE
5 - C	13 - NU
6 - NC	14 - (BL)
7 - USER	15 -

Rm/Rn
0 - P0
1 - P1
2 - A
3 - B
4 - X
5 - PC
6 - SW
7 - SP

W
0 - R/W BYTE
1 - R/W WORD

--> L

L
0 - Rm LOW
1 - Rm HIGH

L
--> 0 - DMA/Rn LOW
1 - DMA/Rn HIGH

S
0 - PASS
1 - SRA
2 - SLL
3 - SRL

FIG. 14

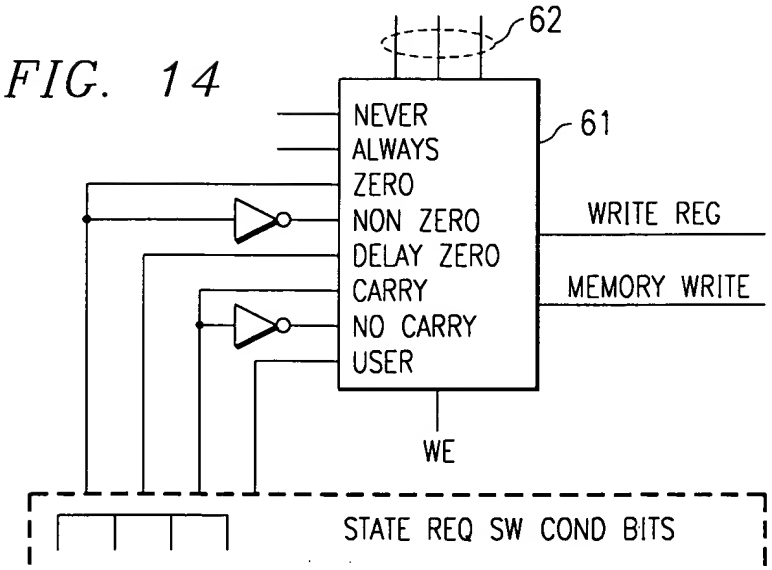
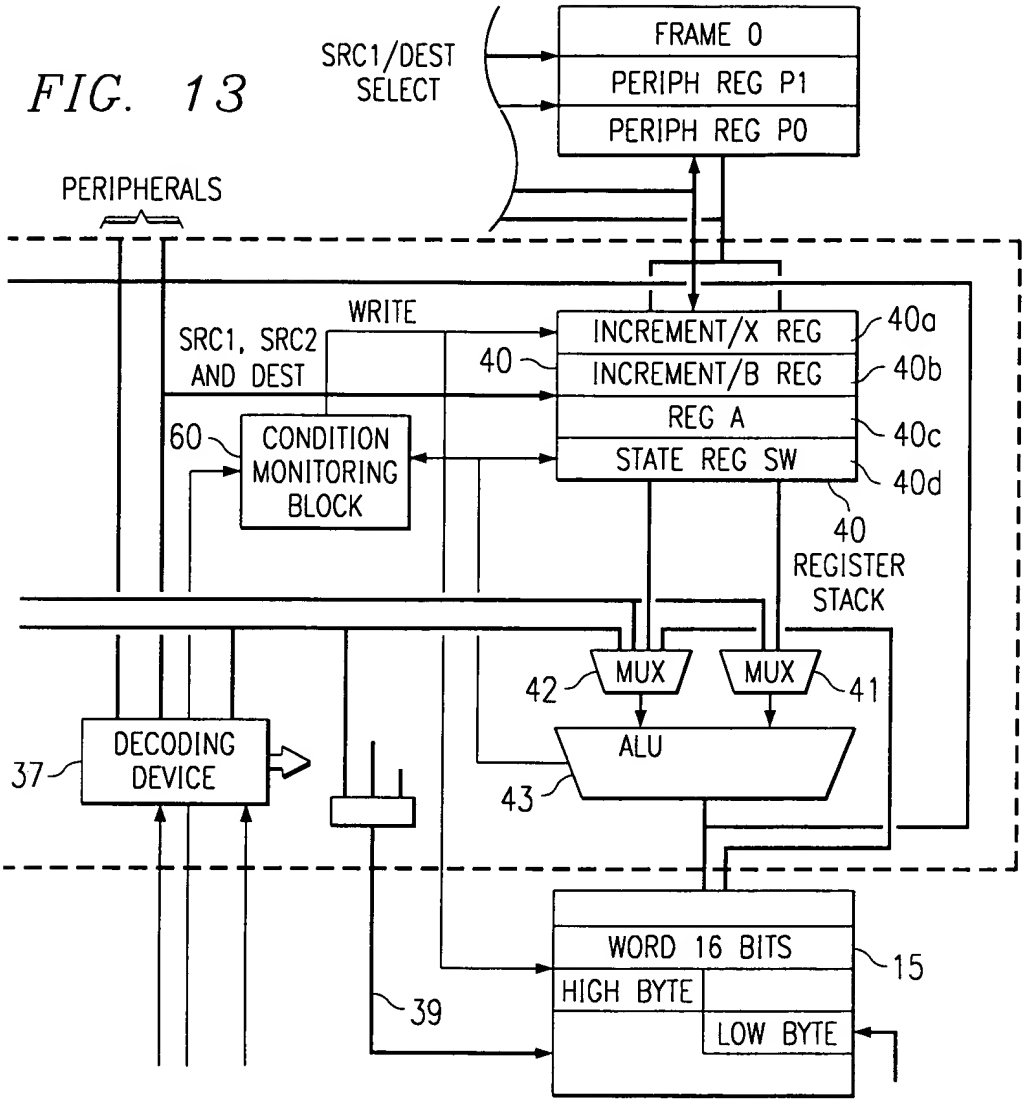


FIG. 13


SRC1/DEST
SELECT
FRAME 0
PERIPH REG P1
PERIPH REG P0
PERIPHERALS
WRITE
SRC1, SRC2
AND DEST
40
INCREMENT/X REG
INCREMENT/B REG
REG A
STATE REG SW
40a
40b
40c
40d
60
CONDITION
MONITORING
BLOCK
40
REGISTER
STACK
42
MUX
MUX
41
ALU
43
37
DECODING
DEVICE
WORD 16 BITS
15
HIGH BYTE
LOW BYTE
39

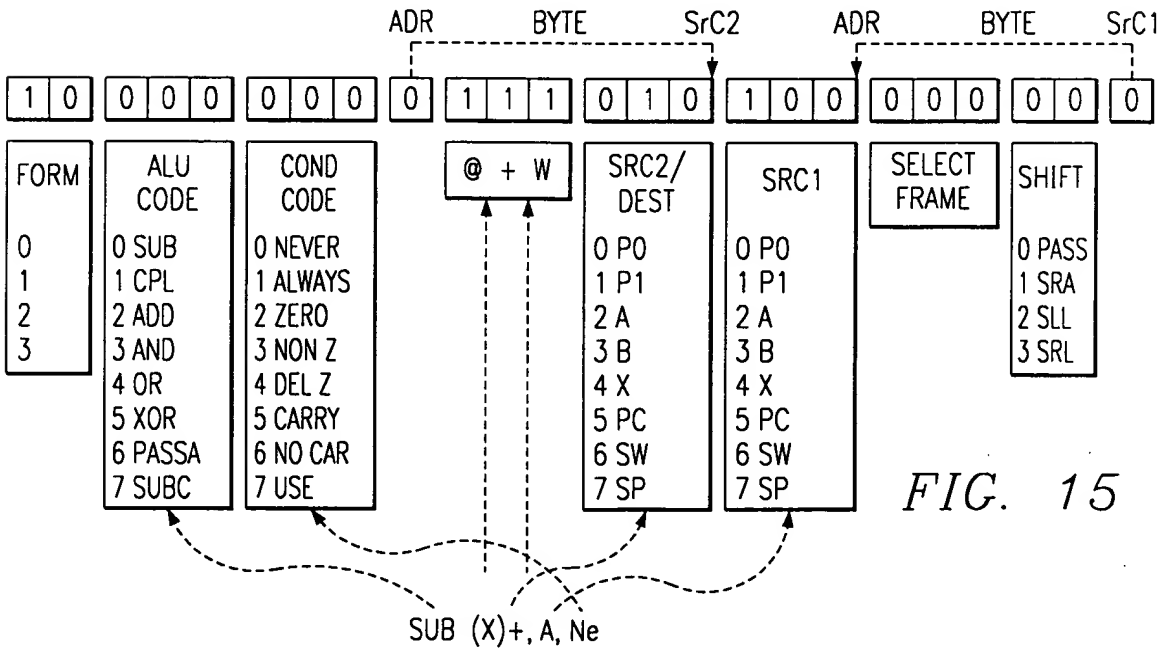

ADR
BYTE
SrC2
ADR
BYTE
SrC1
1 0
0 0 0
0 0 0
0
1 1 1
0 1 0
1 0 0
0 0 0
0 0
0
FORM
0
1
2
3
ALU
CODE
0 SUB
1 CPL
2 ADD
3 AND
4 OR
5 XOR
6 PASSA
7 SUBC
COND
CODE
0 NEVER
1 ALWAYS
2 ZERO
3 NON Z
4 DEL Z
5 CARRY
6 NO CAR
7 USE
@ + W
SRC2/
DEST
0 P0
1 P1
2 A
3 B
4 X
5 PC
6 SW
7 SP
SRC1
0 P0
1 P1
2 A
3 B
4 X
5 PC
6 SW
7 SP
SELECT
FRAME
SHIFT
0 PASS
1 SRA
2 SLL
3 SRL
SUB (X)+, A, Ne

FIG. 15

FIG. 16

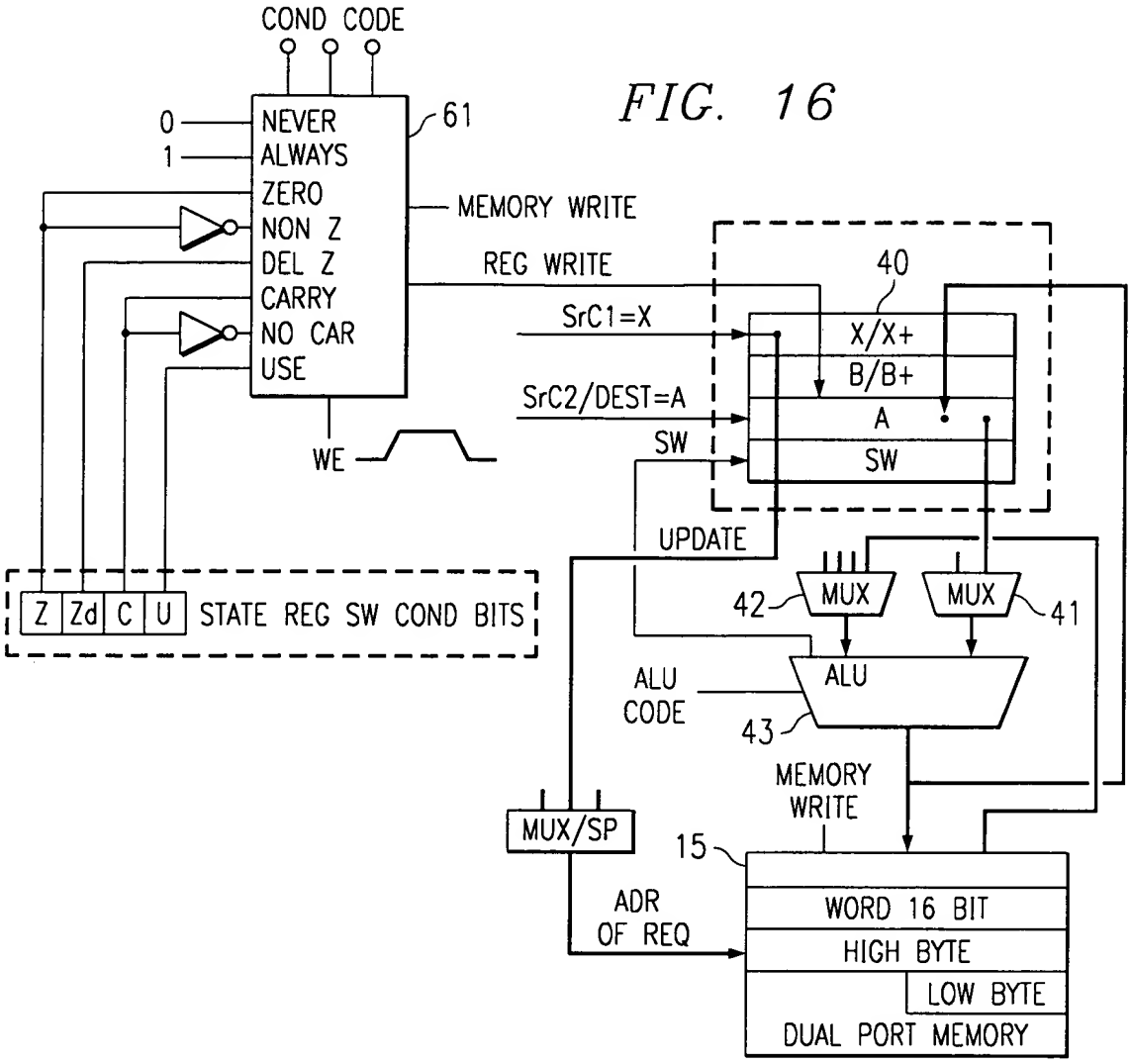
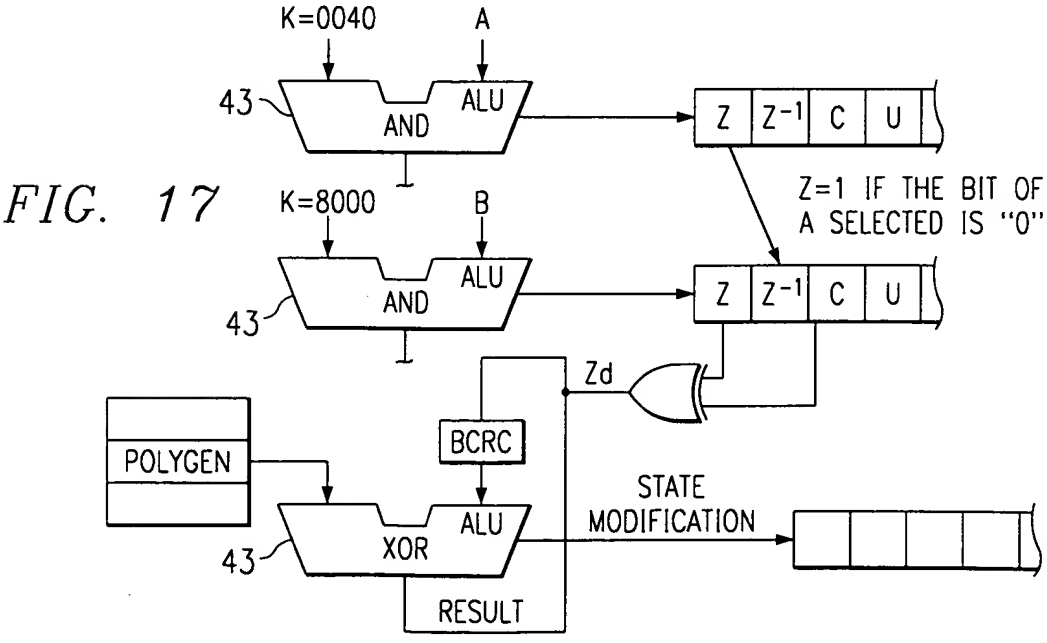

COND CODE
0
1
NEVER
ALWAYS
ZERO
NON Z
DEL Z
CARRY
NO CAR
USE
61
MEMORY WRITE
REG WRITE
WE
SrC1=X
SrC2/DEST=A
SW
40
X/X+
B/B+
A
SW
UPDATE
Z
Zd
C
U
STATE REG SW COND BITS
42
MUX
MUX
41
ALU
CODE
ALU
43
MEMORY
WRITE
MUX/SP
15
ADR
OF REQ
WORD 16 BIT
HIGH BYTE
LOW BYTE
DUAL PORT MEMORY

FIG. 17


K=0040
A
43
AND
ALU
Z
Z-1
C
U
Z=1 IF THE BIT OF
A SELECTED IS "0"
K=8000
B
43
AND
ALU
Z
Z-1
C
U
Zd
POLYGEN
BCRC
43
XOR
ALU
RESULT
STATE
MODIFICATION